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Substitute for form 1449A/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet 1 of 2

Complete if Known


Application Number	10/686,318
Filing Date	October 15, 2003
First Named Inventor	Ware
Art Unit	2818
Examiner Name	Unknown
Attorney Docket Number	RAMB-01042US1

U. S. PATENT DOCUMENTS

[illegible]

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No. ¹	Foreign Patent Document	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T ^d
		Country Code ³ Number ⁴ Kind Code ⁵ (if known)				
WJ		EP0759621	02-26-1997	Ackland et al.	Col. 2, lines 11-19	

Examiner Signature		Date Considered	8/9/04
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PTO/SB/08b (08-03)

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**INFORMATION DISCLOSURE
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Sheet 2

of 2

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Application Number	10/686,318
Filing Date	October 15, 2003
First Named Inventor	Ware et al.
Art Unit	2818
Examiner Name	Unknown
Attorney Docket Number	RAMB-01042US1

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
HW		ISHIBASHI et al., "A 300 MHz 4-Mb Wave-Pipeline CMOS SRAM Using a Multi-Phase PLL", IEEE Journal of Solid-State Circuits, Vol. 30, No. 11, pp. 1189-1195, November 1995	
		NAMBU et al., "A 0.65-ns, 72-kb ECL-CMOS RAM Macro for a 1-Mb SRAM", IEEE Journal of Solid-State Circuits, Vol. 30, No. 4, pp. 491-499, April 1995	
		NAKAMURA et al., "A 220-MHz Pipelined 16-Mb BiCMOS SRAM with PLL Proportional Self-Timing Generator", IEEE Journal of Solid-State Circuits, Vol. 29, No. 11, pp. 1317-1322, November 1994	
		YAMASHITA et al., "A 3.84 GIPS Integrated Memory Array Processor with 64 Processing Elements and a 2-Mb SRAM", IEEE Journal of Solid-State Circuits, Vol. 29, No. 11, pp. 1336-1343, November 1994	
		ISHIBASHI, et al., "FP 18.5: A 300 MHz 4-Mb Wave-Pipeline CMOS SRAM Using a Multi-Phase PLL", IEEE International Solid-State Circuits Conference, pp. 308-309, February 1995	
		TAN et al., "FA 15.1: An 800MHz Quadrature Digital Synthesizer with ECL-Compatible Output Drivers in 0.89m CMOS", IEEE International Solid-State Circuits Conference, pp. 258-259, February 1995	
		YAMASHITA et al., "FA 15.2: A 3.84 GIPS Integrated Memory Array Processor LSI with 64 Processing Elements and 2-Mb SRAM", IEEE International Solid-State Circuit Conference, pp. 260-261, February 1994	

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SignatureDate
Considered

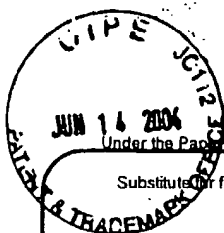
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**INFORMATION DISCLOSURE
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Sheet 1

of

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		Number-Kind Code ² (if known)			
HJ ↓		US-5539696	07-23-1996	Patel	Col. 3, Line 23
		US-5568428	10-22-1996	Toda	Fig. 2D
		US-5644537	07-01-1997	Toda	Fig. 2D
		US-5796660	08-18-1998	Toda	Fig. 2D
		US-6035369	03-07-2000	Ware et al.	
		US-6266737	07-24-2001	Ware et al.	
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		Country Code ³ Number ⁴ Kind Code ⁵ (if known)				
HJ		JP 2159649	06-19-1990	Hiromichi et al	Abstract	✓
HJ		EP 0 655 741 B1	04-28-1999	Toda	Fig. 2D	

Examiner Signature	<i>[Signature]</i>	Date Considered	8/9/04
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